WHAT IS CLAIMED IS:

1. A method for electrically stressing through a specified voltage at least one semiconductor chip on a wafer for controlled contactless burn-in, voltage screen and reliability evaluation of product wafers, said method comprising:

applying said voltage to said at least one chip for the probing thereof in the absence of physically contacting the chip surface; and

magnetically inducing said voltage to said at least one chip through the interposition of a mask onto which the voltage is induced and thereafter conducted to electrical contacts on said wafer.

Sub A1

2. A method as claimed in Claim 1, wherein said applied voltage produces specified voltage bias conditions by inducing the voltage for a circuit utilizing a time varying magnetic field which is fixed with respect to said circuit.

3. A method as claimed in Claim 2, wherein an electrical field which is represented by said induced voltage is based on Faraday's law setting forth that said voltage which is induced by a time rate of change of a magnetic field for said circuit which is fixed with respect to said magnetic field.

4. A method as claimed in Claim 1, wherein said induced voltage is obtained at a top layer of said mask which is positioned on said wafer; and connections are made to said at least one chip by said mask for effectuating said burn-in without interference with the normal operation of said at least one semiconductor chip.

Sub A2

5. A method as claimed in Claim 2, wherein said circuit comprises a loop defining an area on a wafer, said mask being positioned on said wafer so as to enclose said area and having electrical contacts for an induced voltage through said time varying magnetic field within said enclosed area.

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6. A method as claimed in Claim 5, wherein said loop comprises a metallic line on said wafer forming an open circuit having electrical contact points provided at open ends of said circuit for producing said induced voltage.

7. A method as claimed in Claim 6, wherein said loop is of a rectangular configuration to define a generally rectangular area on said wafer.

8. A method as claimed in Claim 6, wherein said metallic line is constituted of copper.

9. A method as claimed in Claim 6, wherein said metallic line is constituted of aluminum.

Sub A3

10. A method as clamed in Claim 2, wherein said circuit comprises a circular magnetic core having an air gap for receiving said wafer with said at least one chip and said mask positioned thereon; and an electrical coil for energizing said magnetic core to produce said specified voltage bias conditions.

11. A method as claimed in Claim 10, wherein said voltage is supplied to said electrical energizing coil from a radio frequency voltage source.

12. A method as claimed in Claim 11, wherein said circular magnetic core is constituted of a Permalloy powder having a composition 2% by weight of *Mo* , 81% by weight of *Ni* with the remainder being iron and impurities.

13. A method as claimed in Claim 10, wherein said air gap receiving said wafer and mask is adapted to provide for the burn-in of differently sized wafers.

14. A method as claimed in Claim 10, wherein said electrical energizing coil consists of an isolated electrical wire comprised of copper wire strands.

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15. A method as claimed in Claim 10, wherein said wafer and mask are retained in said air gap by a wafer holder consisting of a dielectric material.

16. A method as claimed in Claim 10, wherein said magnetic core includes a plurality of said circular magnetic cores interconnected by arms, and each said core having an air gap for receiving respectively a wafer and covering mask so as to facilitate the simultaneous controlled burn-in of a plurality of said wafers.

17. A method as claimed in Claim 2, wherein a rectangular core of non-magnetic material has electrical wire coils wound thereabout, said wire coils being connected to decal masks on a plurality of wafers positioned centrally on said core, each said decal mask being provided to conduct a generated voltage to a chip under said mask.

18. A method as claimed in Claim 17, wherein each said coil is conducted to a time varying voltage source so as to generate a magnetic field perpendicular to the surface of each said wafer in the center of said non-magnetic core.

19. A method as claimed in Clam 18, wherein electrical wires extend from each said mask to a panel for the direct measurements and verification of the direct voltages present on each of said wafer.

20. A method as claimed in Claim 17, wherein said non-magnetic core is constituted of wood.

21. A method as claimed in Claim 17, wherein at least nine wafers are positioned on each core for simultaneous burn-in thereof.

22. A method as claimed in Claim 1, wherein said mask comprises an interposer forming a decal on said wafer surface so as to protect the surface of said wafer from

direct contact with a probe during burn-in and voltage screening through electrical stressing.

23. A method as claimed in Claim 22, wherein said method conducts the generated burn-in voltage to said at least one chip when mountable on P+ silicon substrates.

24. A method as claimed in Claim 22, wherein said method conducts the generated burn-in voltage to said at least one chip when mountable on P- silicon substrates.

25. A method as claimed in Claim 22, wherein said interposer is formed for mounting the wafer on either P+ silicon or P- silicon substrates by the steps of:

fixing a polyimide film to a frame to fully cover said wafer;

depositing at least on layer of a metallic film onto the polyimide film;

patterning said metallic film to provide wiring lines extending to the edge of said wafer to facilitate measuring the induced voltage;

removing exposed metallic layer material at the bottom of the vias and depositing a further wiring line layer forming a ring wire loop on said wafer which is connected to said first wiring lines to facilitate applying an electrical bias to each said ring wire loop;

placing lead/tin bumps into each of said vias and connecting said bumps to said further wiring lines; and

adjusting bump heights whereby the pattern of the bumps interiorly of the decal mask is a mirror-image of wire bond pads or C4 connects on the wafer chip which is to be burned-in.

Sub A4

26. A system for electrically stressing through a specified voltage at least one semiconductor chip on a wafer for controlled contactless burn-in, voltage screen and reliability evaluation of product wafers, said system comprising:

an arrangement for applying said voltage to said at least one chip for the probing thereof in the absence of physically contacting the chip surface; and

magnetically inducing said voltage to said at least one chip through the interposition of a mask onto which the voltage is induced and thereafter conducted to electrical contacts on said wafer.

27. A system as claimed in Claim 26, wherein said applied voltage produces specified voltage bias conditions by inducing the voltage for a circuit utilizing a time varying magnetic field which is fixed with respect to said circuit.

28. A system as claimed in Claim 27, wherein an electrical field which is represented by said induced voltage is based on Faraday's law setting forth that said voltage which is induced by a time rate of change of a magnetic field for said circuit which is fixed with respect to said magnetic field.

29. A system as claimed in Claim 26, wherein said induced voltage is obtained at a top layer of said mask which is positioned on said wafer; and connections are made to said at least one chip by said mask for effectuating said burn-in without interference with the normal operation of said at least one semiconductor chip.

Sub A5

30. A system as claimed in Claim 27, wherein said circuit comprises a loop defining an area on a wafer, said mask being positioned on said wafer so as to enclose said area and having electrical contacts for an induced voltage through said time varying magnetic field within said enclosed area.

31. A system as claimed in Claim 30, wherein said loop comprises a metallic line on said wafer forming an open circuit having electrical contact points provided at open ends of said circuit for producing said induced voltage.

32. A system as claimed in Claim 31, wherein said loop is of a rectangular configuration to define a generally rectangular area on said wafer.

33. A system as claimed in Claim 31, wherein said metallic line is constituted of copper.

34. A system as claimed in Claim 31, wherein said metallic line is constituted of aluminum.

Sub A6

35. A system as clamed in Claim 27, wherein said circuit comprises a circular magnetic core having an air gap for receiving said wafer with said at least one chip and said mask positioned thereon; and an electrical coil for energizing said magnetic core to produce said specified voltage bias conditions.

36. A system as claimed in Claim 35, wherein said voltage is supplied to said electrical energizing coil from a radio frequency voltage source.

37. A system as claimed in Claim 36, wherein said circular magnetic core is constituted of a Permalloy powder having a composition 2% by weight of *Mo*, 81% by weight of *Ni* with the remainder being iron and impurities.

38. A system as claimed in Claim 35, wherein said air gap receiving said wafer and mask is adapted to provide for the burn-in of differently ~~sized~~ wafers.

39. A system as claimed in Claim 35, wherein said electrical energizing coil consists of an isolated electrical wire comprised of copper wire strands.

40. A system as claimed in Claim 35, wherein said wafer and mask are retained in said air gap by a wafer holder consisting of a dielectric material.

41. A system as claimed in Claim 35, wherein said magnetic core includes a plurality of said circular magnetic cores interconnected by arms, and each said core having an air gap for receiving respectively a wafer and covering mask so as to facilitate the simultaneous controlled burn-in of a plurality of said wafers.

42. A system as claimed in Claim 27, wherein a rectangular core of non-magnetic material has electrical wire coils wound thereabout, said wire coils being connected to decal masks on a plurality of wafers positioned centrally on said core, each said decal mask being provided to conduct a generated voltage to a chip under said mask.

43. A system as claimed in Claim 42, wherein each said coil is conducted to a time varying voltage source so as to generate a magnetic field perpendicular to the surface of each said wafer in the center of said non-magnetic core.

44. A system as claimed in Clam 43, wherein electrical wires extend from each said mask to a panel for the direct measurements and verification of the direct voltages present on each of said wafer.

45. A system as claimed in Claim 42, wherein said non-magnetic core is constituted of wood.

46. A system as claimed in Claim 42, wherein at least nine wafers are positioned on each core for simultaneous burn-in thereof.

47. A system as claimed in Claim 26, wherein said mask comprises an interposer forming a decal on said wafer surface so as to protect the surface of said wafer from

direct contact with a probe during burn-in and voltage screening through electrical stressing.

48. A system as claimed in Claim 47, wherein said method conducts the generated burn-in voltage to said at least one chip when mountable on P+ silicon substrates.

49. A system as claimed in Claim 47, wherein said method conducts the generated burn-in voltage to said at least one chip when mountable on P- silicon substrates.

50. A system as claimed in Claim 47, wherein said interposer is formed for mounting the wafer on either P+ silicon or P- silicon substrates by means of:

fixing a polyimide film to a frame to fully cover said wafer;

depositing at least on layer of a metallic film onto the polyimide film;

patterning said metallic film to provide wiring lines extending to the edge of said wafer to facilitate measuring the induced voltage;

removing exposed metallic layer material at the bottom of the vias and depositing a further wiring line layer forming a ring wire loop on said wafer which is connected to said first wiring lines to facilitate applying an electrical bias to each said ring wire loop;

placing lead/tin bumps into each of said vias and connecting said bumps to said further wiring lines; and

adjusting bump heights whereby the pattern of the bumps interiorly of the decal mask is a mirror-image of wire bond pads or C4 connects on the wafer chip which is to be burned-in.

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